

AMENDMENTS TO THE CLAIMS

1. **(Currently amended)** An antifuse device for an integrated circuit formed on a substrate, the antifuse device comprising:

a first layer of magnetic material formed on an exposed surface of the substrate;
a second layer of magnetic material positioned above the first layer;
a dielectric layer interposed between the first layer and the second layer wherein the first layer, the second layer and the dielectric layer form an MTJ junction; and
a ~~logic~~ first circuit that is selectable so as to interconnect the first layer to a first electrical potential such that the first and second layers of magnetic material are shorted together when the ~~logic~~ first circuit is selected, wherein the shorting of the first and second layers of magnetic material is selected to affect the logical outcome of a logical circuit of an electrical device in a manner so as to achieve a desired circuit configuration of the electrical device.

2. **(Original)** The device of Claim 1, wherein the first layer comprises a pinned layer of magnetic material that is magnetized in a first fixed direction, the second layer comprises a soft layer of material that can be magnetized in either the first fixed direction or a second direction, and the dielectric layer comprises a tunnel dielectric layer interposed between the first layer and the second layer.

3. **(Original)** The device of Claim 2, wherein the first layer comprises a layer of NiFe that is approximately 100 – 500 Å thick, the second layer comprises a layer of NiFe that is approximately 40 – 50 Å thick, and the dielectric layer comprises a layer of Al₂O₃ that is approximately 10 – 15 Å thick.

4. **(Original)** The device of Claim 2, wherein the antifuse device has a resistance of greater than approximately 1 MegaOhm prior to the interconnection to the first electrical potential and wherein the antifuse device, upon interconnection to the first electrical potential is shorted across the tunnel dielectric layer.

5. **(Original)** The device of Claim 4, wherein the selected voltage is approximately 1.8 volts.

6. **(Original)** The device of Claim 1, wherein the antifuse MTJ device further comprises a first barrier layer, a pinning layer, and a second barrier layer.

7. **(Original)** The device of Claim 6, wherein the first barrier layer comprises a layer of Ta that is approximately 50 Å thick, the pinning layer comprises IrMn that is

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approximately 100 Å thick, and the second barrier layer comprises Ta that is approximately 200 Å thick.

Claims 8-16 (**Cancelled**)